



# SIGNAL

## Newsletter

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## Ribbon-Cutting Launches New Samsung RFIC Design Center in Technology Square

**ATLANTA** (August 17, 2005) — Officials from the Samsung Electro-Mechanics Company (SEM), the state of Georgia and the Georgia Institute of Technology held a ribbon-cutting August 17 for the company's new North American radio frequency integrated circuit (RFIC) design center. The center will initially be located in the Technology Square Research Building, which also houses the GEDC.

The Samsung RFIC Design Center will develop technology for next-generation communication systems, expanding to system-on-chip devices for modem, digital and RF equipment. Innovations developed by researchers at the new center will impact a broad spectrum of Samsung's worldwide product offerings.

Over the next five years, the new center could employ more than 100 design scientists and engineers.

In April, the company announced its decision to open the center in Atlanta, citing Georgia Tech's strengths in radio-frequency and mixed-signal research as major reasons for choosing the location. Center researchers are expected to collaborate with Georgia Tech faculty and staff on a broad range of issues, including contributions to the IEEE standard for cognitive radio (IEEE 802.22).

Chang-Ho Lee, formerly with the GEDC, has been named director of the new design center. Dr. Lee has become one of the top young scientists in mixed signal technology.

Joy Laskar, GEDC's director, expects the collaboration with Samsung to boost the center's expertise and reputation in the areas of high-frequency, high-speed electronic design, and the utilization of new technology in next generation communication applications.

"We are excited at the prospect of working with SEM Co. to pursue areas of common interest," he said. "We appreciate the confidence the company has shown through the location of the new design center with the GEDC."



(Left to right) Mike Cassidy, president of the Georgia Research Alliance; Ho-Moon Kang, CEO of Samsung; Jean-Lou Chameau, provost of Georgia Tech, and Byeong-Cheon Koh, chief technical officer of Samsung, pause in front of the entrance to the new Samsung design center in the Technology Square Research Building building in Atlanta.

## Pirelli Chooses Atlanta for New Headquarters

**ATLANTA** (September 23, 2005) — Officials of Italian-based Pirelli and the Georgia Institute of Technology have signed a five-year strategic research and development agreement. Together they will develop new broadband access technologies including high-frequency and optical systems.

Pirelli and researchers from the Georgia Electronic Design Center (GEDC) at Georgia Tech will develop a new generation of integrated optical systems. Atlanta will become the North American operational branch of Pirelli Labs, the advanced research center of the group based in Milan. The group, founded in 2001, specializes in broadband access and second generation photonics.

Pirelli will also consolidate all North American corporate staff activities in the new Atlanta center, including the headquarters of Pirelli Broadband Solutions, a new company that engineers and markets the innovations conceived in Pirelli Labs. This alliance will help position Georgia to become a world-class center of research excellence in photonics and broadband technologies.

Pirelli's location in Atlanta will initially include laboratory space at the GEDC in the Technology Square Research Building at Georgia Tech, as well as additional headquarters office space next door in the Centergy One building.

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Georgia Tech welcomed Pirelli to Technology Square September 22. Shown (L-R) are Joy Laskar, director of the Georgia Electronic Design Center; Kevin Riddett, president and chief executive officer of Pirelli North America Inc.; Jean-Lou Chameau, Georgia Tech provost and vice president of academic affairs, and Gary S. May, chair of the Georgia Tech School of Electrical and Computer Engineering. Here Chameau presents an award to Riddett, as Laskar and May stand by.



## Executive Summary

We have had a number of exciting things happening at the Georgia Electronic Design Center (GEDC) in the past several months since our last IAB meeting.

Last month Georgia Gov. Sonny Perdue announced that the Pirelli Group, a major international player in the communications and automotive industries, will be moving its North American Headquarters to Georgia Tech’s Technology Square complex. Pirelli will also open a broadband research laboratory in the Technology Square Research Building (TSRB) that houses GEDC.

In August, Georgia Tech, the state of Georgia and GEDC celebrated the arrival of the Samsung Electro-Mechanics Company to TSRB, as Samsung formally opened its new North American Center of Excellence in Radio Frequency Integrated-Circuit (RFIC) design center.

Both new centers will collaborate with GEDC research teams. Over the next five years, these centers are expected to employ well over 100 design scientists and engineers.

Several GEDC researchers have recently received awards for their outstanding work. Prof. David Anderson, a member of GEDC’s

analog-research team, received the Presidential Early Career Award for Scientists and Engineers this year. Gerald DeJean, an electrical engineering doctoral student under the guidance of Prof. Manos Tentzeris in the GEDC, recently won a two-year Microsoft fellowship to continue his research. And two GEDC faculty received the rank of IEEE Fellow in their work related to integrated circuits and communications.

GEDC researchers continue to win major new awards with Intel, Raytheon, National Semiconductor, DARPA, NSF, NASA and others. One such award from NASA to Prof. John Papapolymerou and Prof. Manos Tentzeris provides \$551,000 over three years for research that includes electronically scannable antenna arrays as well as a new approach to multilayer packaging for ICs, MEMS, passives and other components.

In order to better serve our members, we have initiated a testbed renovation plan within our current facilities to make sure that we maintain our state-of-the-art technological edge. The renovations include the addition of a new Millimeter-Wave testbed and a separate Optical testbed, which will be used to support our new and future GEDC members.

They join our existing 3G Wireless, Mixed Signal and Ubiquitous Wireless Network testbeds.

The industry continues to progress rapidly, and we are well positioned to be part of that growth and excitement. Now more than ever it is critical that we continue to communicate and work together so that our efforts can be channeled in directions that will most meaningfully affect your future success. GEDC looks forward to continuing as an important strategic partner to our member companies.



Best Regards,

Dr. Joy Laskar

*Director, Georgia Electronic Design Center*

*Joseph M. Pettit Professor of Electronics*

## GTAC Summary

Two years ago the Georgia Tech Analog Consortium (GTAC) joined GEDC in the Technology Square Research Building. That decision has made a major impact on our work – and how we work. Bringing faculty, students and industry together in one place has proved to be a powerful strategy.

As the center of excellence for analog IC circuits and systems design, we fit well with GEDC’s focus on total system design. Within GEDC we have been able to maintain our traditional analog-signal-processing focus and bring together many faculty with research directions on analog circuits and systems.

At the same time we also work side by side with researchers in computer engineering,

digital ICs, and systems design. And we connect with industry and its needs and viewpoints.

Such collaboration is bearing fruit. Georgia Tech faculty member David Anderson, a GTAC/GEDC researcher, recently won the Presidential Early Career Award for Scientists and Engineers (PECASE) as well as an NSF CAREER award totaling \$400,000 for analog signal-processing research. Prof. Anderson and I also recently won a two-year DARPA contract totaling some \$900,000 to study circuits and systems for CMOS image processing.

Analog has an important role to play in the mixed signal-processing approach to the por-

table wireless devices of tomorrow. Analog chips typically use about one thousand times less power than digital ICs to do the same job. That’s the difference between a battery lasting two hours or lasting for a month.

Such possibilities are exciting to a researcher. And working at GEDC has given us the collaborative infrastructure to help bring such visions to reality.

Cordially,

Dr. Paul Hasler

*Director, Georgia Tech Analog Consortium*

*Associate Professor, Georgia Tech School of Electrical and Computer Engineering*

## PECASE Winner David Anderson Envisions an Analog-Digital Future

by Rick Robinson

For his work in analog signal processing, David V. Anderson won the prestigious Presidential Early Career Award for Scientists and Engineers (PECASE) in 2005 – and an NSF CAREER award totaling \$400,000 shortly before that.

The awards are helping Anderson and his team at the Georgia Electronic Design Center (GEDC) as they develop new generations of analog signal-processing chips and integrated circuits. Such research could make possible a wide range of future mobile devices that are smaller, more effective and flexible, and less power-hungry than current technology.

"Analog processing is not new – it preceded digital processing," says Anderson, an associate professor in Georgia Tech's School of Electrical and Computer Engineering (ECE). "But at Georgia Tech we have made it much more powerful, so that complicated operations can be performed in analog systems."

GEDC scientists study mixed-signal processing, which involves integrated circuits that use both digital and analog technologies. Anderson himself works in both fields. Analog chips are especially useful, he explains, because they're typically smaller and use far less power than digital chips, thereby conserving batteries and reducing heat.

Analog circuits may also be preferred for many tasks suited to mobile devices, including speech recognition, audio processing, and image and video processing. Moreover, using analog chips can decrease the cost of a system by reducing the need to translate analog signals – such as voice or images – into a digital format.

One of Anderson's main research concentrations involves reconfigurable analog systems. The technical name for this capability is a field programmable analog array (FPAA). Unlike older FPAAs, those being developed at GEDC are large, fully interconnected chips that can handle a variety of sophisticated functions.

Traditionally, analog systems have had their functions hard-wired into them, while digital systems changed functions by simply switching software. Anderson's team is enabling analog circuits to switch between tasks by altering their memories in way that is analogous to the digital world.

Analog memories, Anderson explains, can be made to resemble the flash memory used today in flash drives and other devices. Analog devices can be reconfigured using what he calls analog floating gates. Using this technique, an analog chip performing speech recognition could be quickly reprogrammed to clean up an audio signal instead.

"There are many opportunities in this area and not many other players," he says.

Eventually, this kind of small, low-power, intelligent technology could show up in a raft of products, including cell phones, surveillance equipment, watches with speech-recognition capability, and self-adjusting hearing aids.

"It's important for these systems to be very robust," Anderson says. "It's one thing to have speech recognition work on an office computer with the same speaker and microphone – it's quite another thing to make it work in a restaurant or a car or with a child's voice. Those environments are very difficult."

Georgia Tech in signal processing. His work has led to several patents related to audio signal processing, including development of a digital-hearing aid algorithm that became a successful commercial product.

Anderson emphasizes that he's only one member of Georgia Tech's analog-research team. At GEDC, he works closely with Paul E. Hasler, another associate professor in ECE, and their respective doctoral students. Together they form the Cooperative Analog and Digital Signal Processing Laboratory, one of several groups that Anderson works with in GEDC and in ECE.

Hasler and his students design analog chips, while Anderson and his students work on analog-chip circuits and the software algorithms they use.

"It's a very synergistic relationship around here," Anderson says. "Georgia Tech provides a unique atmosphere and opportunity for the type of cross-disciplinary collaboration that has made this area of research possible,"

In researching signal processing, Anderson often turns to the natural world for ideas.

"I often look at human biological functions as inspiration for developing signal processing algorithms and hardware architecture," Anderson says. "I have always been interested in how and why humans do so much better than computers at sensory tasks."

In general, he explains, nature does well with all manner of "imperfect computation" that would stump digital computers. Biological systems can solve a complicated problem by doing many simple computations.

Computers, Anderson believes, may soon have to approach problems in a similar piecemeal way. Today's super-fast CPUs are becoming unacceptably hot. The future may belong to multiple core architectures – computers with many CPUs that each receive different parts of a given problem. Such multiple-core architectures demand new programming skills, but may be the best way to get around the performance wall that computers are beginning to hit.

Anderson earned an undergraduate and a master's degree in electrical engineering from Brigham Young University in 1993 and 1994. In 1999, he received a doctorate from



David Anderson stands immediately to the left of President George W. Bush, as the president makes a point to PECASE winners assembled in the Oval Office.

## Microsoft Awards Prestigious Fellowship to Student Working at GEDC

Gerald DeJean, a Georgia Tech graduate student in the School of Electrical and Computer Engineering, is one of 12 young U.S. and Canadian scientists to win a prestigious two-year Microsoft Research Graduate Fellowship.

DeJean is an electrical engineering student associated with the Georgia Electronic Design Center (GEDC).

"I feel really good about getting this award," said DeJean. "This funding will help me further my work in the design and development of wideband compact antennas and antenna arrays in planar or multilayer technologies for telecom, space and millimeter-wave applica-

tions. I will have the opportunity to collaborate with some of the best minds in RF design as well as researchers in other fields such as materials science and physics."

DeJean is advised by Prof. Emmanouil Tentzeris, a Georgia Tech associate professor who heads the ATHENA research group and is one of the founding faculty of the High-Frequency Research Lab of GEDC.

DeJean is a doctoral candidate in the ATHENA group, which is part of the High-Frequency Lab at the GEDC. The ATHENA group explores both advances in electromagnetic simulator technologies and its applications to the design and optimization of modern RF/Microwave systems.

"Gerald fully deserved this prestigious award for his breakthrough work in the area of compact planar antennas for WLAN and RFID applications," Tentzeris said. "He is one of the

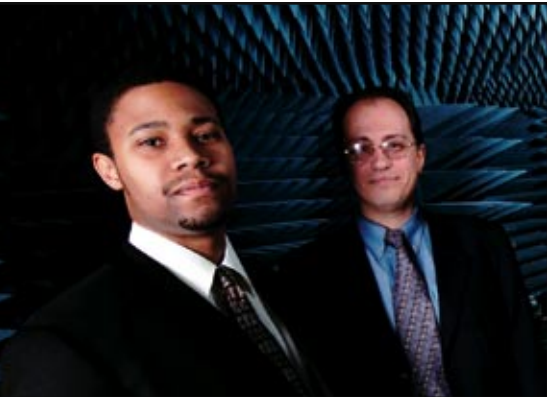
smartest students I've ever had, and I expect he soon will be one of the young rising stars in the antenna research area."

DeJean, a resident of Los Angeles, holds a master's degree in electrical engineering from Georgia Tech. He received a bachelor's in electrical engineering from Michigan State University in 2001.

Joy Laskar, director of the GEDC, said DeJean's award reflects the level of GEDC's work in high-frequency high-speed electronic design and utilization of new technology in next generation communication applications.

"Gerald is representative of the gifted young scientists we see here at GEDC," Laskar said. "We are proud of his achievements."

DeJean traveled to Seattle to compete for the fellowship with more than 100 other applicants. This year's other Microsoft award winners come from a variety of United States and Canadian universities that include the Massachusetts Institute of Technology, Stanford University, the University of British Columbia, the University of California Berkeley, the University of Toronto and the University of Washington.



*Gerald DeJean, left, a graduate student who recently won a prestigious fellowship from Microsoft Corp., is pictured here with his adviser, Prof. Emmanouil Tentzeris of the Georgia Tech School of Electrical and Computer Engineering. Both men pursue research at the Georgia Electronic Design Center.*

## Laskar and Harris Chosen as IEEE Fellows

Joy Laskar, director of the Georgia Electronic Design Center, and GEDC researcher H. Michael Harris were recently elected 2005 IEEE Fellows.

Each year the IEEE Fellow Committee recommends a select group of recipients for the award. In conferring the honor, the Fellow Committee cited Laskar's contributions to the modeling and development of high frequency communication modules. Harris received the honor for contributions to the electrical and thermal properties of wide bandgap semiconductors.

Laskar, who is also Joseph M. Pettit Professor of Electronics in Georgia Tech's School of Electrical and Computer Engineering, said he was very pleased by news of the award.

"Being elected a Fellow is one of the IEEE's highest honors, and I am gratified to be distinguished by the Institute in this way," Laskar said.

The IEEE is a leading organization for the advancement of technology. Its global association consists of members who are engineers, scientists and allied professionals. Their technical interests are centered on the electrical and computer sciences, and in engineering and

related disciplines.

The IEEE's two predecessor societies – the American Institute of Electrical Engineers and the Institute of Radio Engineers – were founded in 1884 and 1912, respectively. The two organizations united in 1963 to form the IEEE, which now comprises more than 365,000 members in about 150 countries.



H. Michael Harris



Dr. Joy Laskar

"Attracting first-class research and development facilities from global leaders like Samsung, a company known for its forward-looking leadership in the industry, is precisely what the GEDC was established to do By leveraging Georgia Tech's research and educational assets, we can work with private industry to build Georgia's economy based on the technology industries of the future."

Wayne Clough, PRESIDENT, GEORGIA INSTITUTE OF TECHNOLOGY

## NASA Awards \$551K to GEDC Researchers

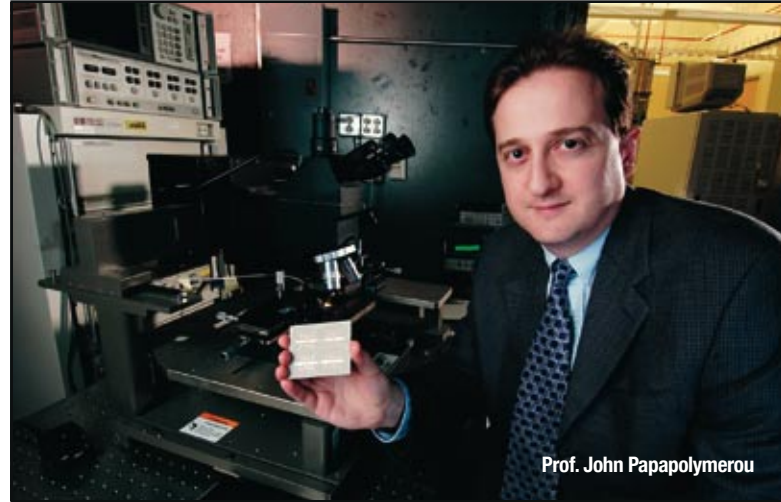
Prof. John Papapolymerou and Prof. Manos Tentzeris, researchers associated with the Georgia Electronic Design Center (GEDC), recently received a substantial multi-year award to continue work in several areas of component research.

NASA awarded the scientists \$551,000 over three years for research that includes electronically scannable antenna arrays, and a new approach to multilayer packaging for ICs (integrated circuits), MEMS, passives and other components utilizing a low-cost, homogeneous dielectric substrate material.

The new award extends a three-year contract that Papapolymerou and Tentzeris received from NASA in 2002. The work conducted at

GEDC under this contract by the two researchers and their graduate-student teams has already resulted in two patents pending, with other patents applied for, and in numerous conference papers and scientific-journal publications.

Potential applications for the new discoveries include portable wireless devices, space and military uses.



Prof. John Papapolymerou

## Tentzeris Wins IEEE Outstanding Young Engineer Award

Prof. Manos M. Tentzeris, a GEDC researcher and an associate professor in the Georgia Tech School of Electrical and Computer Engineering, has been awarded the 2006 IEEE Microwave Theory and Techniques Symposium (MTT-S) Outstanding Young Engineer of the Year Award.

This competitive award honors an outstanding young MTT-S member under the age of 39, and is given to one person from the academic world each year. It differs from other MTT-S achievement-based awards because it recognizes a person, not an achievement.

Prof. Tentzeris was specifically recognized by MTT-S for innovation in the development of multi-resolution CAD tools and in the design and optimization of 3D RF modules in ceramic (e.g. LTCC) and organic (e.g. LCP) substrates up to millimeter-wave frequency range.

The Outstanding Young Engineer of the Year includes a cash award and other honors to be given at the annual IEEE MTT-S International Microwave Symposium 2006 in San Francisco, Calif.

At GEDC, Tentzeris' research includes RF antenna design, MEMS, RF/wireless 3D inte-

gration and packaging. He heads Adaptive Techniques for Hybrid Electromagnetic Numerical Applications (ATHENA), a group of 15 researchers. He is one of the founding faculty of GEDC's High-Frequency Research Lab.



Prof. Manos M. Tentzeris

### Georgia Electronic Design Center Georgia Institute of Technology

85 Fifth Street, N.W.

Atlanta, Georgia 30308 USA

[www.gedcenter.org](http://www.gedcenter.org)

[info-gedc@gedcenter.org](mailto:info-gedc@gedcenter.org)

404.894.1400

### Pirelli *continued from page 1*

Under the agreement, visiting researchers from both organizations will work in Georgia Tech laboratories—and in the clean rooms of Pirelli Labs near Milan. There, advanced facilities devoted to research and development of optical components for telecommunications occupy about 54,000 square feet in the Pirelli Labs building.

Pirelli's initial team will consist of executive, engineering, scientific, marketing and sales professionals. Pirelli, a pioneer in photonics worldwide, is among the world's leaders and innovators in a number of fields, including its key markets of tires and telecommunications systems.

## GEDC Laboratories

### High-Frequency (HF) Systems Lab

The 1,400-square foot HF Lab is the cornerstone of the hardware device research underway within the Georgia Electronic Design Center. The mission of the HF Lab is to develop and combine new technologies with the help of leading-edge industry to perform research relevant to industry, provide enhanced manufactured products and new capabilities.

Essentially, the High Frequency Lab is an aggregation of six related research teams working together to solve pressing next generation communications design challenges. Expertise within this lab includes physics, fabrication, testing, device verification and circuits and systems characterization. Each HF researcher addresses new challenges by generating new performance-enhancing concepts and applying them toward next generation "macro-scale items," i.e., products manufactured for consumer use.

Researchers in the lab develop the following technologies: System-on-a-Package, Mixed-Signal Verification, Emerging Device Technologies, System-on-a-Chip, and MEMS and Antenna Design.

### High Speed Digital Lab

Researchers in this lab examine the trend towards mixed signal integration using System-on-Chip and System-on-Package solutions. Projects include signal and power integrity, CAD tools and electromagnetic interference (EMI).

This team's signaling objective is to achieve 10 Gbps high throughput via chip-to-chip communication and solve the global interconnect problem. Its solution includes using highly resistive Silicon for minimum loss; 50/100 micrometer solder bumps for low inductance, low loss board materials, high density lines with thin dielectrics for shielding and realizing seamless transitions from package-chip-package.

Its power objective is to support 281 W at 0.6 V with SSN < 5 % VDD. Its solution includes eliminating a first level package to lower

inductance, 50/100 micrometer solder bumps for low inductance, using high density packages with through vias to lower inductance, embedded decoupling and isolation of core and I/O.

Its design objective is to develop next generation tools for mixed signal design. Its solution includes time and frequency domain electromagnetic methods, reduced order modeling and measurement-based outcome.

The group developed three mixed-signal SOP test beds to investigate EMI.

### Network Portable Platform and Appliances Lab

This lab is focused on a low cost network-enabled thermostat controller for real-time monitoring and control of home temperature via the Internet, as well as the development of novel algorithms for Call Admission Control in Next Generation Wireless Systems (4G). Researchers are also developing a general messaging application, Smart Networked Appliance Platform Technology (SNAPTECH), and Embedded Software for Telemedicine Applications.

Deliverables include the production of software applications that will increase productivity at low cost and less energy, among them:

- Design and implementation of an Operating Service Architecture (OSA) porting networked smart appliances (TV, DVD, home PCs, smart phones, smart meters, smart cards, smart homecare devices, etc.) and integration into appliance platforms that plug into a broadband residential network.
- Build a universal user interface between home users and smart appliances at home through our proprietary Set-top Box (STB) as both a centralized controlling device as well as a residential gateway that combines the TV with multiple Internet services. The research emphases and research challenges include: addressing research issues in networked appliance platforms; developing networked appliance technologies; and integrating a great variety of protocol stacks utilized in smart appliances in a smart home environment.

Develop innovative applications on smart STB as a centralized controlling device and a gateway in a residential network. These value-added applications to STB work on top of OSA and the middleware developed for OSA.

### Computer-Assisted Design Lab

A lab containing 30 advanced workstations running state-of-the-art computer assisted design (CAD) and simulation software. The high speed processors, many machines feature multi-processors, and advanced visualization capacities of these workstations enable the design of innovative, complex, high-performance, cutting-edge microwave equipment.

Designers in the lab develop the following technologies: modeling and design of advanced circuits and modules, circuit layouts and mask design, electromagnetic simulations, design tool development, layout optimization and package design

### Cooperative Analog/Digital Signal Processing Lab

This team examines combinations of programmable analog signal processing and digital signal processing techniques for real world processing. Because real-world signals are analog while much of the modern control and communication is digital, these researchers seek the "where" -- where to partition the analog-digital boundary so that the overall functionality of a system is enhanced. A superset of mixed-signal research, CADSP allows freedom of movement for the partition between analog and digital computations by focusing tightly on algorithms as well as circuit implementation. When adding functionality to analog systems, these experts enhance the capabilities of the controlling digital system, and therefore, the entire product under consideration.

The range of applications for these approaches reaches from auditory and speech processing to beam-forming, multidimensional signal processing, radar computations,

"We are excited at the reception we have received in Georgia and the cooperation at all levels from the governor, his staff and the university system." **Kevin Riddett, PRESIDENT AND CHIEF EXECUTIVE OFFICER OF PIRELLI NORTH AMERICA INC.**

communications processing, and image processing and recognition.

## Ultrafast Optical Communications Lab (UFOCL)

The efforts of the Ultrafast Optical Communications Group are dedicated to the design, fabrication, and implementation of devices and subsystems for single-wavelength optical data transmission at rates exceeding 100 Gbps. The UFOCL research group focuses on a wide range of topics in optical fiber communications and related technologies. Research interests include short pulse generation and characterization, high-speed optoelectronic devices and links, and mitigation of fiber-induced signal impairments arising from nonlinearities and dispersion.

This technology enables:

- integrated electro-optic devices without performance impairment
- integrated control of phase and amplitude of optical signals
- advanced modulation formats exploiting phase, commonly seen in wireless
- interferometric transmitters and receivers
- integrated detection at communication wavelength via use of InN detectors
- monitoring of extinction ratio
- dynamic chirp control
- pulse shaping

## Pirelli Broadband Solutions Laboratory

Under a recently signed agreement, Pirelli and researchers from GEDC will develop a new generation of integrated optical systems. Atlanta will become the North American operational branch of Pirelli Labs, an advanced research center based in Milan, Italy, that specializes in broadband access and second generation photonics.

Together with GEDC researchers, visiting researchers from Pirelli Labs will combine their expertise in photonics research and electronic design to develop new generations

of opto-electronic devices and next generation photonic testbeds. Research results from the Pirelli Broadband Solutions Laboratory will influence domestic and international standards on optical communications.

## Samsung RFIC Design Center

Samsung Electro-Mechanics Company's new North American radio frequency integrated circuit (RFIC) design center has been established in the Technology Square Research Building that also houses GEDC.

Georgia Tech faculty and staff collaborate with the Samsung RFIC Design Center researchers on a broad range of issues, including contributions to the IEEE standard for cognitive radio (IEEE 802.22).

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## Sun/Dell/Agilent Training Center

The purpose of the 50-station Sun/Dell/Agilent Training Center is to provide an educational platform for simulations of circuit designs. The training rooms provide capabilities for simulation and layout of advanced integrated circuits as well as full-wave 3-D simulations for passive and active integration. Industry will access the room to provide training to faculty and students on new applications and testing applications.



**Georgia Electronic Design Center  
Georgia Institute of Technology**

### Member Companies

Agilent  
Anadigics  
Asahi  
Ardext  
Barco  
Broadcom  
Cermet  
CIENA  
Cisco Systems  
Eagleware  
Echostar  
EG Technologies  
Engent  
GTronix  
HP Labs  
IBM  
IDT  
Intel  
iVivity  
Jacket Micro Devices  
Kipper Technologies  
Motorola  
Movaz Networks  
Nanoventions  
National Semiconductor  
nGimat  
Nortel Networks  
Optical Fiber Solutions  
Pirelli  
Proxim Corporation  
Quellan  
Raytheon  
Samsung (S.A.I.T.)  
Samsung Electro-Mechanics  
Siemens  
SoC Solutions  
Sun Microsystems  
UXPi  
VeriSign  
Vocalocity  
Wave7Optics

## Speakers Announced for Upcoming Industry Advisory Board Meeting

Jerry Bautista, Linda P.B. Katehi, Richard Lai and John Zolper will deliver keynote addresses at the GEDC Industry Advisory Board meeting in Atlanta Oct. 24-25. Because of their common industry membership and mission, the Georgia Electronic Design Center and the Georgia Tech Analog Consortium are jointly sponsoring the meeting.



### Jerry Bautista

Director of Technology Management  
Intel Microprocessor Research  
Laboratory



Dr. Jerry Bautista is Director of Technology Management for Intel's Microprocessor Research Laboratory. In addition, he has led several corporate strategic technology groups including Fiber to the Home; high volume low cost optical interconnect modules, and most recently memory/interconnect bandwidth challenges/solutions for server and client platforms. He also served the CTO function for Intel's planar optical waveguide efforts. Before joining Intel, he held the position of CTO at WaveSplitter for three years. Prior to that he held a series of positions at Lucent Technologies. He received a bachelor's degree from Stanford and a PhD from Princeton, both in chemical engineering.

### Linda P.B. Katehi

John A. Edwardson Dean of Engineering  
Purdue University



Prof. Linda Katehi joined the faculty of the EECS Department of the University of Michigan, Ann Arbor, in 1984, and was promoted to professor in 1994. In January 2002 Katehi joined Purdue University

as the John A. Edwardson Dean of Engineering and as professor of electrical and computer engineering. Katehi has received numerous awards, including the IEEE Marconi Prize in 2000 and the IEEE MTT-S Distinguished Educator Award in 2002. She is a Fellow of IEEE. She received the B.S.E.E. degree from the National Technical University of Athens, Greece in 1977, and the M.S.E.E. and Ph.D. degrees from the University of California, Los Angeles, in 1981 and 1984 respectively.

### Richard Lai

Microelectronic Technology Department  
Northrop Grumman



Dr. Richard Lai has nearly 20 years experience in research, development and production of advanced GaAs-based and InP-based HEMT device and MMIC RF technologies. Since 1994 he has been the principal investigator for advanced HEMT research and development at Northrop Grumman in Redondo Beach (formerly TRW). In 2001 he became manager of the Microelectronics Technology Department, which is responsible for development of all microelectronics products, and in 2002 became a Northrop Grumman technical fellow.

He has authored or co-authored more than 100 total papers, patents and conference presentations involving advanced GaAs and InP-based device and circuit technology. He received a Ph.D. degree from University of Michigan, Ann Arbor, in 1991.

### John Zolper

Director, Microsystems  
Technology Office  
DARPA



Dr. John C. Zolper was appointed Director of DARPA's Microsystems Technology Office (MTO) in March 2005. He is responsible for research projects directed by the MTO Program Managers and for conceptual planning in the areas of electronics, photonics, MEMS, component architectures, and algorithms. Prior to being appointed MTO Director, he was Deputy Office Director from September 2002. He first joined the MTO in October 2001 as a Program Manager. He is the author or co-author of over 150 journal and conference papers and seven book chapters. He is a Senior Member of IEEE. He received a PhD in electrical engineering from the University of Delaware in 1987 and a bachelor's degree in physics from Gettysburg College in 1982.